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EXAMINER	
WASHBURN, DOUGLAS N	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,154	LIU, YEN-FU	
	Examiner	Art Unit	
	Douglas N. Washburn	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-12, 14-19 and 21-27* is/are rejected.

7)☒ Claim(s) *7,13,20 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1 Claims 6 and 7 are objected to because of the following informalities:

Claim 6, line 2 "...the BIST circuit..." lacks antecedance;

Claim 7, line 4 "...the BIST circuit..." lacks antecedance;

Examiner suggests "...a BIST circuit...".

Correction is required.

Claim Rejections - 35 USC § 102

2 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-12, 14-19 and 21-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Ober et al. (US 6,708,273) (Hereafter referred to as Ober).

Ober teaches:

Taking test vector data as input to an integrated circuit to produce response data as output in regard to claim 1

(e.g. column 5, lines 10-15);

Using a one-way-hash function to transform response data into a test message digest in regard to claim 1

(e.g. column 5, lines 10-15);

Verifying a test message digest against a standard message digest to determine whether the test message digest meets a predetermined requirement in regard to claim 1

(e.g. column 5, lines 10-15);

A test message digest is verified by comparing the test message digest with a standard message digest in regard to claim 2

(e.g. column 5, lines 10-15);

A one-way-hash function is SHA-1 performed by a SHAX in regard to claim 3

(e.g. column 5, lines 26-40; column 6, lines 4 and 5; figure 1, element 6);

A one-way-hash function is MD5 in regard to claim 4

(e.g. column 6, lines 4 and 5);

A one-way-hash function is performed by a one-way-hash hardware circuit in regard to claim 5

(e.g. column 2, lines 39-41; figure 1, element 30);

A one-way-hash hardware circuit is embedded as part of a BIST circuit in an integrated circuit in regard to claim 6

(e.g. column 78, lines 45-51; figure 1, element 6);

A one-way-hash hardware circuit is implemented within automated test equipment in regard to claim 8

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash function is performed by a specifically designed single chip in automated test equipment in regard to claim 9

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash function is performed by a microprocessor in automated test equipment in regard to claim 10

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash function is performed by a DSP in automated test equipment in regard to claim 11

(e.g. column 1, lines 27-30; figure 1, element 2);

Taking test vector data as input to a standard integrated circuit and producing a standard response data as output in regard to claim 12

(e.g. column 5, lines 10-15);

Using a one-way-hash function to transform standard response data into a standard message digest in regard to claim 12

(e.g. column 5, lines 10-15);

A standard integrated circuit is verified to be faultless before a standard message digest is generated in regard to claim 12

(e.g. column 5, lines 10-15);

Automated test equipment for sending test vector data to an integrated circuit producing response data in response to test vector data and for receiving a test message digest to be verified against a standard message digest to determine whether the test message digest meets a predetermined requirement in regard to claim 14

(e.g. column 5, lines 10-15);

A one-way-hash module for receiving response data and performing a one-way-hash function to generate a test message digest in regard to claim 14

(e.g. column 6, lines 4-12);

A comparator for comparing a test message digest with a standard message digest in regard to claim 15

(e.g. column 161, lines 25-28);

A one-way-hash module is a SHAX performing SHA-1 in regard to claim 16

(e.g. column 5, lines 26-40; column 6, lines 4 and 5);

A one-way-hash module performs MD5 in regard to claim 17

(e.g. column 6, lines 4 and 5);

A one-way-hash module is a one-way-hash hardware circuit in regard to claim 18

(e.g. column 2, lines 39-41; figure 1, element 30);

A one-way-hash hardware circuit is embedded as part of a BIST circuit in an integrated circuit in regard to claim 19

(e.g. column 78, lines 45-51);

A one-way-hash hardware circuit is implemented within automated test equipment in regard to claim 21

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash hardware circuit is a specifically designed single chip in automated test equipment in regard to claim 22

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash module is represented by a code and programmed in a microprocessor in automated test equipment in regard to claim 23

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash to function is performed by a DSP in automated test equipment in regard to claim 24

(e.g. column 5, lines 11-15; figure 1, elements 2);

A main module for producing response data in response to test vector data from automated test equipment in regard to claim 25

(e.g. column 1, lines 27-30; figure 1, element 2);

A one-way-hash module for receiving response data and performing a one-way-hash function to generate a test message digest to be sent to automated test equipment in regard to claim 25

(e.g. column 1, lines 27-30; figure 1, element 30);

A test message digest is verified against a standard message digest to determine whether the test message digest meets a predetermined requirement in automated test equipment in regard to claim 25

(e.g. column 1, lines 27-30);

A one-way-hash module is a SHAX performing SHA-1 in regard to claim 26

(e.g. column 5, lines 26-40; column 6, lines 4 and 5; figure 1 element 6);

And a one-way-hash module performs MD5 in regard to claim 27

(e.g. column 6, lines 4 and 5).

Allowable Subject Matter

3 Claim 7 would be allowable if rewritten to overcome the objection, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 13, 20 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Claim 7 recites, in part, "said integrated circuit comprises a plurality of IP blocks and a plurality of one-way-hash hardware circuits are respectively embedded in corresponding IP blocks as part of the BIST circuit in said IP blocks". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 13 recites, in part, "simulating behavior of said integrated circuit as well as said one-way-hash function in a computer and generating said standard message digest in response to said test vector data". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 20 recites, in part, "said integrated circuit comprises a plurality of IP blocks and a plurality of one-way-hash hardware circuits are respectively embedded in corresponding IP blocks as part of the BIST circuit in said IP blocks". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 28 recites, in part, "said integrated circuit comprises a plurality of IP blocks and a plurality of one-way-hash modules are respectively embedded in corresponding IP blocks as part of a BIST circuit in said IP blocks, and wherein each of said IP blocks comprises a main module". This feature in combination with the remaining claimed structure avoids the prior art of record.

It is these limitations, which are not found, taught or suggested in the prior art of record, and are recited in the claimed combination that makes these claims allowable over the prior art.

Conclusion

4 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas N. Washburn whose telephone number is (571) 272-2284. The examiner can normally be reached on Monday through Thursday 6:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRYAN BUI
PRIMARY EXAMINER

DNW